High-Performance Inductors

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***Abstract*—In this paper, we describe the design, test data, and analysis of several circular spiral inductors fabricated on GaAs substrates using the multifunction self-aligned gate multilayer process. Various factors such as high inductance, high-quality Q, high current handling capacity, and compactness are studied. Several configurations for inductors were investigated to optimize the inductor geometry such as the linewidth, spacing between the turns, conductor thickness, and inner diameter. It includes measured effects of various parameters on inductor performance, such as linewidth, spacing, inner diameter, metal thickness, underlying dielectric, and dielectric thickness. It is shown experimentally that the Q factor of spiral inductors can be enhanced by using 9-μm-thick metallization and placing inductors on a 10-μm-thick polyimide layer, which is placed on top of the GaAs substrate. Using this technique, we have observed up to 93% improvement in the Q factor of circular spiral inductors, as compared to standard spiral inductors fabricated on GaAs substrates. Inductors having thick metallization can also handle dc currents as large as 0.6 A.**

***Index Terms*—High-current inductors, improved Q, monolithic inductors, multilayer inductors, spiral inductors.**

I. Introduction

THE emergence of wireless and mobile applications along with increased phased-array applications is relentlessly driving efforts to reduce monolithic-microwave integrated-circuit (MMIC) cost. Lumped-element design using inductors, capacitors, and resistors is a key technique for reducing MMIC chip area, resulting in more chips per wafer, and leading to higher yields and lower cost. Currently available inductors [1]–[6] are not always suitable to these applications due to limitations in inductance per unit area, current handling capacity, and unloaded Q factor.

Multilayer polyimide MMIC technologies employing multilevels of metallization are finding increasing applications in compact and high-performance circuits. One can also develop very high-density MMICs using multilevel inductors. Using a multilayer polyimide process, we have designed over 50 single-level test inductors to study experimentally the inductor characteristics such as the Q factor, self-resonance frequency ($f_{\rm res}$), inductance per unit area, and current handling capacity. Results of this investigation are presented in this paper.

II. Inductor Design

Both square and circular spiral inductors are being used in microwave integrated circuits (MICs) and MMICs. It has been reported [7], [8] that the circular geometry has about 10%–20% higher Q and $f_{\rm res}$ values than the square configuration. In this paper, we will describe only circular spiral inductors, however, wherever possible for comparison purposes, square spiral inductors will be discussed.

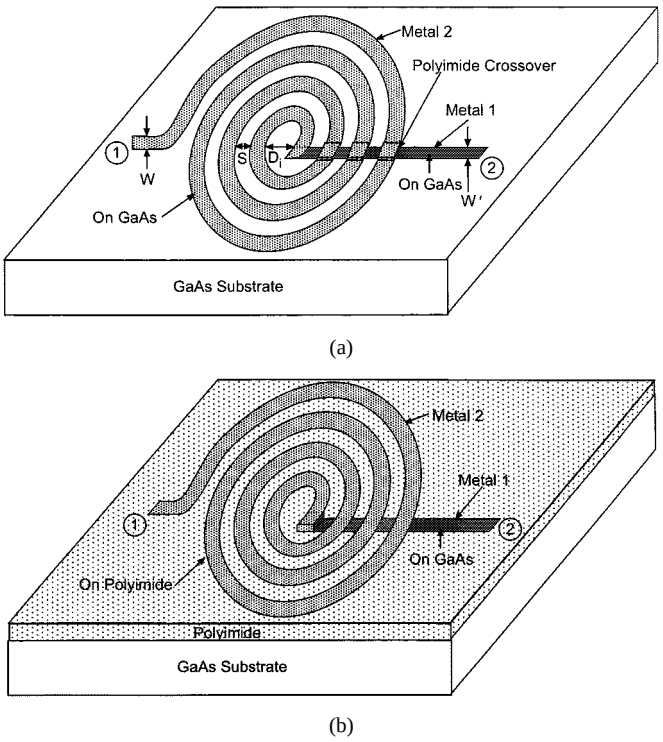

Fig. 1. Circular spiral inductors. (a) Standard. (b) Multilayer.

We have designed several types of circular spiral inductors having different dimensions such as the linewidth, spacing between the turns, and inner diameter. These inductors (Fig. 1) were fabricated using a standard and multilayer MMIC process and different conductor thicknesses. A summary of these inductors is given in Table I, including the dimensions (Figs. 1(a) and 2) and current handling capability of several inductors studied in this paper. In the inductor column, the first three characters show the number of turns (e.g., 2.5), the fourth character (i.e., I) designates that the coil inductor has circular geometry, the fifth character as a numeric designator represents the inductor's dimensions (W, S, W', Di), and the last character signifies its fabrication using polyimide layers and multilevel conductors: standard-S, inductor conductor on 3-μm polyimide—A and B, conductors on 10-μm polyimide and multilevel plating—M and conductors on 10-μm polyimide, and thick multilevel plating—T. Using the multilayer process, we studied two types of low-loss and high current handling inductors for integrated circuits (ICs) compatible with multifunction self-aligned gate (MSAG) GaAs monolithic process [9]. The first type of inductor is designed using a single level of plating. In this case, as shown in Fig. 1(b),

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TABLE I
SUMMARY OF VARIOUS INDUCTORS WITH DIMENSIONS AND CURRENT HANDLING CAPACITY. FOR DIMENSIONAL LABELS REFER TO FIGS. 1 AND 2

Inductor #	# of Turns n	Dimensions (μm)								Current Handling* (mA)
		W	S	Di	W′	t_1	t_2	d_1	d_2	
1.5I1S	1.5	20	8	108	20	0.6	4.5	0	3	40
1.5I1A	1.5	20	8	108	20	1.5	4.5	0	3	100
1.5I1B	1.5	20	8	108	40	1.5	4.5	0	3	200
1.5I1M	1.5	20	8	108	20	4.5	4.5	3	7	300
1.5I1T	1.5	20	8	108	40	4.5	9.0	3	7	600
2.5I1S	2.5	16	10	108	16	0.6	4.5	0	3	32
2.5I1A	2.5	16	10	108	16	1.5	4.5	0	3	80
2.5I1B	2.5	16	10	108	32	1.5	4.5	0	3	160
2.5I1M	2.5	16	10	108	16	4.5	4.5	3	7	240
2.5I1T	2.5	16	10	108	32	4.5	9.0	3	7	480
3.5I1S	3.5	12	14	108	12	0.6	4.5	0	3	24
3.5I1A	3.5	12	14	108	12	1.5	4.5	0	3	60
3.5I1B	3.5	12	14	108	24	1.5	4.5	0	3	120
3.5I1M	3.5	12	14	108	12	4.5	4.5	3	7	180
3.5I1T	3.5	12	14	108	24	4.5	9.0	3	7	360
3.5I5S	3.5	8	8	50	8	0.6	4.5	0	3	16
3.5I5A	3.5	8	8	50	8	1.5	4.5	0	3	40
3.5I5B	3.5	8	8	50	16	1.5	4.5	0	3	80
3.5I5M	3.5	8	8	50	8	4.5	4.5	3	7	120
3.5I5T	3.5	8	8	50	16	4.5	9.0	3	7	240

*Based on 3×10^5 amp/cm^2 current density

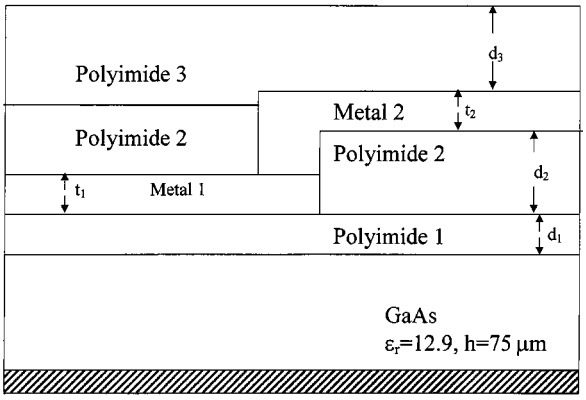

Fig. 2. Cross-sectional view of the multilayer inductor. For multilayer process $t_1 = t_2 = 4.5$ μm and $d_1 = 3$ μm, and $d_2 = d_3 = 7$ μm.

the inductor pattern with thick plated metallization 2 is placed on 3-μm-thick polyimide layer backed by 75-μm GaAs substrate. The inner most turn of the conductor is connected to the output line through a via in the 3-μm polyimide layer 1 and metallization 1. The metallization 1 is about 1.5-μm thick and placed on the GaAs substrate. Parameters for these inductors are listed in Table II. Fig. 3 shows some of 2.5–turn inductors studied in this paper. All inductor patterns are drawn to the same scale. In the second type of inductors, two levels of plating are used. The first conductor layer is placed on 3-μm-thick polyimide and it connects the inner most turn of the inductor to the output line through the via. The second conductor layer is placed on 7-μm-thick polyimide and forms the inductor pattern. The total polyimide thickness under the inductor pattern is about 10 μm. Both metallizations are 4.5-μm thick and are connected by a via in the 7-μm-thick polyimide. Fig. 2 shows the multilayer structure used for multilayer inductors.

We also designed several compact inductors having various number of turns (1.5, 2.5, 3.5, 4.5, and 5.5). All these inductors have inner mean radius of 50- and 8-μm linewidth and 8-μm spacing between the turns. Metal 1, which is placed on GaAs, has a thickness of 1.5 μm, whereas metal 2, having thickness of 4.5 μm, is placed on 3-μm polyimide. They are of types A and B. The only difference between types A and B is that, in type-A inductors, $W' = W$ (Fig. 1) and in type-B inductors, $W' = 2W$.

Inductors fabricated using two levels of plating can be designed for much higher current capacity than is possible if one wiring layer must be thin, as is the case if only one layer of plating is available. Along with increased current capability, the Q factor is enhanced due to lower resistance. The current handling capability of a conductor is limited by the onset of electromigration. The conductor thickness and linewidth determine the current carrying capacity of the inductor. A safe value of maximum current density of gold conductors on a flat surface is 3.3×10^5 A/cm^2. For example, for a 4.5-μm-thick conductors, the calculated maximum current handling capacity is 15-mA/μm-wide line. Table I provides the calculated value of maximum current handling for several inductors investigated in this study.

III. FABRICATION

The fabrication process used in the manufacture of these inductors is the MSAG standard and multilayer plating process

TABLE II
MODEL PARAMETER VALUES FOR TYPE A INDUCTORS

Inductor #	Inductor Type	# of Turns	Dimensions (μm)			R_{dc} (Ω)	R_{ac} (Ω)	R_d (Ω)	L_1 (nH)	L_2 (nH)	L (nH)	C_{ga} (pF)	C_{gb} (pF)	C_1 (pF)	C_2 (pF)	f_{res} (GHz)	Peak Q_{eff}
			W	S	Di												
1.5I0A	X0	1.5	20	8	50	0.1	0.167	0.001	0.0001	0.0001	0.378	0.019	0.020	0.0001	0.00001	>40	49
1.5I1A	X1	1.5	20	8	108	0.18	0.15	0.009	0.0001	0.0001	0.563	0.028	0.027	0.0001	0.00001	37.6	52
1.5I2A	X2	1.5	20	8	158	0.23	0.16	0.018	0.0001	0.0001	0.760	0.038	0.036	0.0001	0.00001	27.2	48
1.5I3A	X3	1.5	20	8	210	0.24	0.24	0.02	0.092	0.077	0.85	0.048	0.046	0.0001	0.00001	22.3	40.5
1.5I4A	X4	1.5	12	8	50	0.10	0.19	0.0001	0.0001	0.0001	0.342	0.014	0.011	0.0001	0.00001	>40	41.5
1.5I5A	X5	1.5	8	8	50	0.20	0.155	0.01	0.0001	0.0001	0.32	0.010	0.008	0.00002	0.00001	>40	35
2.5I0A	X0	2.5	16	10	50	0.20	0.3	0.03	0.18	0.30	0.42	0.020	0.033	0.002	0.0096	28.7	37
2.5I1A	X1	2.5	16	10	108	0.30	0.25	0.06	0.16	0.10	1.10	0.039	0.037	0.0016	0.0043	21.00	39
2.5I2A	X2	2.5	16	10	158	0.35	0.27	0.1	0.21	0.23	1.45	0.048	0.054	0.0045	0.0045	16.2	38
2.5I3A	X3	2.5	16	10	210	0.38	0.3	0.15	0.24	0.26	1.91	0.059	0.065	0.0023	0.0052	13.15	35.5
2.5I4A	X4	2.5	12	8	50	0.25	0.33	0.021	0.028	0.029	0.751	0.022	0.021	0.00002	0.00001	34.2	35
2.5I5A	X5	2.5	8	8	50	0.25	0.40	0.02	0.033	0.032	0.696	0.019	0.015	0.00003	0.00005	38.1	30.0
3.5I0A	X0	3.5	12	14	50	0.38	0.55	0.06	0.32	0.32	1.18	0.036	0.039	0.0048	0.0075	18.7	30.0
3.5I1A	X1	3.5	12	14	108	0.45	0.52	0.13	0.26	0.29	2.08	0.047	0.053	0.0001	0.006	14.0	31.5
3.5I2A	X2	3.5	12	14	158	0.6	0.7	0.17	0.30	0.33	3.00	0.061	0.071	0.0001	0.0025	10.6	29.5
3.5I3A	X3	3.5	12	14	210	0.7	0.80	0.25	0.37	0.48	3.74	0.073	0.082	0.0003	0.0032	8.75	27.5
3.5I4A	X4	3.5	12	8	50	0.3	0.55	0.06	0.033	0.44	1.12	0.022	0.037	0.016	0.0001	20.5	30.0
3.5I5A	X5	3.5	8	8	50	0.3	0.60	0.07	0.036	0.034	1.407	0.023	0.023	0.001	0.0018	25.0	27.5
4.5I0A	X0	4.5	12	14	50	0.46	0.66	0.12	0.33	0.34	2.36	0.053	0.066	0.002	0.008	11.9	30.0
4.5I5A	X5	4.5	8	8	50	0.4	0.8	0.16	0.044	0.036	2.421	0.029	0.033	0.0023	0.002	17.5	25.5
5.5I5A	X5	5.5	8	8	50	0.5	1.0	0.21	0.047	0.038	3.64	0.044	0.054	0.0029	0.002	11.8	25.0

used in M/A-COM Inc.'s MMIC and radio-frequency integrated-circuit (RFIC) production. The multilayer process features two levels of global 4.5-μm plated gold metallization. Polyimide is used as an interlevel dielectric for the interconnect metal and a glassivation or buffer layer for mechanical protection of the finished circuitry. The polyimide layers are fabricated using automated coating and curing equipment. Patterning is accomplished using thick photoresist masks and reactive ion etching in oxygen. The thickness for the interlevel layers 1, 2, and buffer layer polyimide are 3, 7, and 7 μm, respectively. The thickness of the plated gold metallizations 1 and 2 are about 4.5 and 4.5 μm. Thicker (10 μm) metallization 2 is also available for the M/A-COM Inc.'s MMIC process. The separation between the two plated metallizations is about 7 μm and they are connected together by vias through 7-μm polyimide. In the standard process, the thicknesses of metals 1 and 2 are 0.6 or 1.5 and 4.5 μm, respectively, and 3-μm polyimide is used as an interlevel dielectric for crossovers [see Fig. 1(b)]. Test data reported in this paper was taken for inductors fabricated on a 75-μm-thick GaAs substrate. The GaAs substrate thickness tolerance is ± 5 μm. Polyimide tolerances are $\pm 1\mu$m in thickness and ± 0.1 in the dielectric constant value. Characteristics of the polyimide material used in our production process are listed in Table III.

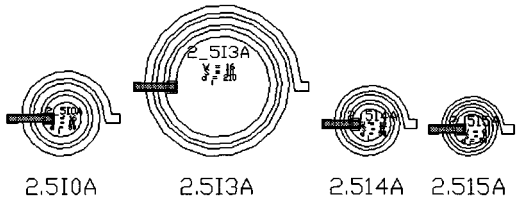

Fig. 3. Four different types of 2.5-turn inductors. 2.5I0A: $W = 16$, $S = 10$, $Di = 50$, 2.5I3A: $W = 16$, $S = 10$, $Di = 210$, 2.5I4A: $W = 12$, $S = 8$, $Di = 50$, and 2.5I5A: $W = S = 8$, $Di = 50$. All dimensions are in micrometers.

TABLE III
PROPERTIES OF POLYIMIDE MATERIAL

Dielectric constant = 3.2
Loss tangent = 0.005
Dielectric strength = 430 V/μm
Thermal conductivity = 0.002 W/cm°C
Coeffcient of thermal expansion
= 6.5 X 10^{-6}/°C in *x*-and-y direction
= 70 x 10^{-6}/°C in *z*-direction

IV. INDUCTOR MODEL AND THE FIGURE-OF-MERIT

Various methods for modeling and characterization of spiral inductors have been described in the literature [10]–[18]. The inductors are characterized by its inductance value, the unloaded Q factor, and its resonant frequency $f_{\rm res}$. The two-port lumped-element equivalent-circuit model used to characterize these inductors is shown in Fig. 4. The series resistance R used to model the dissipative loss is given by

$$R = R_{\rm dc} + R_{\rm ac}\sqrt{f} + R_d f \tag{1}$$

where $R_{\rm dc}$ represents dc resistance of the trace, and $R_{\rm ac}$ and R_d represent model resistances due to skin effect, eddy current excitation, and dielectric loss in the substrate. In the model L_t $(L + L_1 + L_2)$, R and C's represent the total inductance, series resistance, and parasitic capacitances of the inductor, respectively. The frequency f is expressed in gigahertz.

There is no unique definition of the Q factors for printed inductors, which can be used over a broad microwave frequency range. Several different definitions of Q factors for inductors

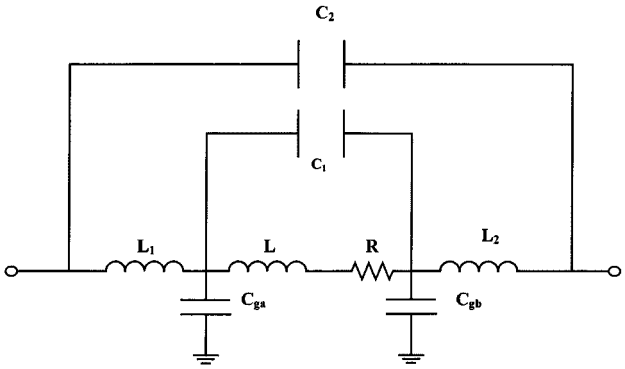

Fig. 4. Lumped-element equivalent-circuit model of the inductor.

have been used in the literature [13]–[21]. The most general definition of Q is based on ratio of energy stored, W_S to energy dissipated, W_D in the inductor per cycle, i.e.,

$$Q = \frac{W_S}{W_D}. \tag{2}$$

At low frequencies ($f \ll f_{\rm res}$), inductor's primary reactance is inductive and

$$Q = \frac{\omega L_t}{R}. \tag{3}$$

When the inductor is used as a resonant component close to its self-resonance frequency $f_{\rm res}$, a more appropriate definition of the Q factor is in terms of 3-dB bandwith (BW) given by

$$Q = \frac{f_{\rm res}}{\rm BW}. \tag{4}$$

There is another definition of the Q factor, which has been used for distributed resonators, and is evaluated from the rate of change of input reactance with frequency [22], [23]

$$Q = \frac{f_{\rm res}}{2R}\left[\frac{dX_{\rm in}}{df}\right] \tag{5}$$

where $X_{\rm in}$ is the input reactance of the inductor and $dX_{\rm in}/df$ is determined at $f_{\rm res}$.

In microwave circuits where the inductors are used far below the self-resonance frequency, the degree at which the inductor deviates from an ideal component is described by the effective Q factor $Q_{\rm eff}$, expressed as follows [6], [15], [16], [18]–[21]:

$$Q_{\rm eff} = \frac{{\rm Im}[Z_{\rm in}]}{{\rm Re}[Z_{\rm in}]} = \frac{X}{R} \tag{6}$$

where ${\rm Re}[Z_{\rm in}]$ and ${\rm Im}[Z_{\rm in}]$ are the real and imaginary parts of the input impedance of a spiral inductor, respectively. This definition leads to an unusual condition that $Q_{\rm eff}$ becomes zero at resonance. Since in RF and microwave circuits, for series applications of inductors, the operating frequencies are well below the self-resonance frequency, the above definition is traditionally accepted [21], and is used throughout the paper to compare several types of spiral inductors described here.

The $Q_{\rm eff}$-factor values were obtained by converting two-port S-parameters data into one-port S-parameters by placing a perfect short at the output port. In this case, the following relationships were used to calculate the Q factor and $f_{\rm res}$:

$$\Gamma_{\rm in} = S_{11} - \frac{S_{12}S_{21}}{1+S_{22}} \tag{7}$$

and

$$Z_{\rm in} = 50\frac{1-\Gamma_{\rm in}}{1+\Gamma_{\rm in}} = R + jX \ (\Omega). \tag{8}$$

The self-resonant frequency ($f_{\rm res}$) of an inductor is calculated when ${\rm Im}[Z_{\rm in}] = 0$, i.e., the inductive reactance and parasitic capacitive reactance become equal. At this point, ${\rm Re}[Z_{\rm in}]$ is maximum and the angle of $Z_{\rm in}$ changes sign. The inductor's first resonance frequency is of a parallel resonance type. Beyond the resonant frequency, the inductor becomes capacitive.

For a given inductance value, one would like to have the highest possible $Q_{\rm eff}$ and $f_{\rm res}$ in the smallest possible area of an inductor. In an inductor changing W, S and the inner diameter affects its area and it is difficult to have good comparison. Here, we define a unique figure-of-merit of an inductor (FMI) as follows:

$${\rm FMI} = \frac{Q_{\rm eff}\cdot f_{\rm res}}{\text{Inductor Area}}. \tag{9}$$

Thus, a highest FMI value is desirable.

V. Test Data and Discussions

We tested several inductors for two-port S-parameters up to 40 GHz using RF probes. Measured data was taken using an on-wafer thru-reflect line (TRL) deembedding technique. The TRL calibration standards were placed directly on the same GaAs substrate carrying the inductor structures so that the same calibration standards can be used for all multilayer inductors. From the deembedded S-parameter data, the model element values were derived and the $Q_{\rm eff}$ factor and $f_{\rm res}$ were obtained, as described in the previous section. The $Q_{\rm eff}$ values are obtained at a maximum $Q_{\rm eff}$-point frequency, which is experimentally observed at about $(1/2)f_{\rm res}$. Table II summarizes typical model parameter values for various circular spiral inductors tested on a 75-μm-thick GaAs substrate. The inductors are classified into six groups, depending upon the $W+S$ dimension and the inner diameter. Fig. 5 shows the total inductance as a function of inductor area for inductor type A. Higher inductance and area for a given inductor type mean more number of turns. The description of six groups of inductors is as follows:

$X0$ have Di =50 and $n = 1.5 \quad W = 20, S = 8$
n =2.5 $\quad W = 16 \quad S = 10$
n =3.5 $\quad W = 12 \quad S = 14$
n =4.5 $\quad W = 12 \quad S = 14$

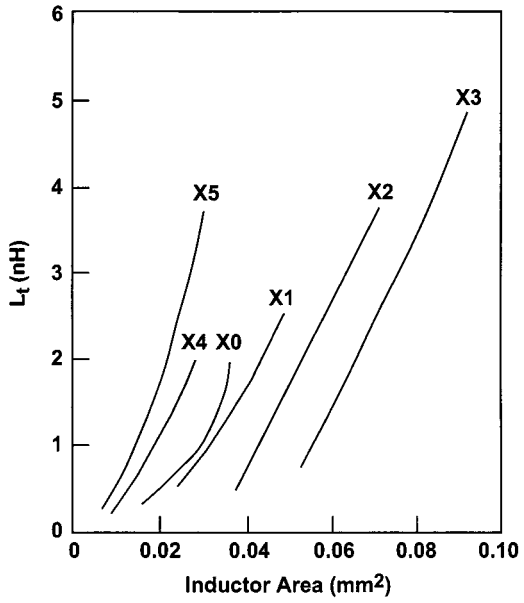

Fig. 5. Variations of measured total inductance versus area for different inductors of type A.

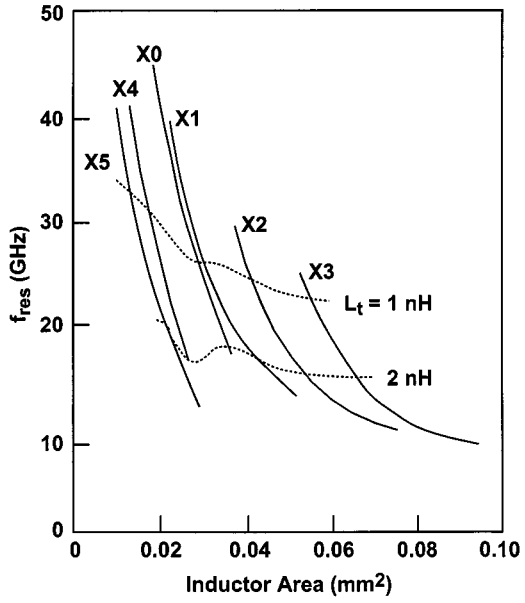

Fig. 7. Variations of measured self-resonance frequency versus area for different inductors of type A.

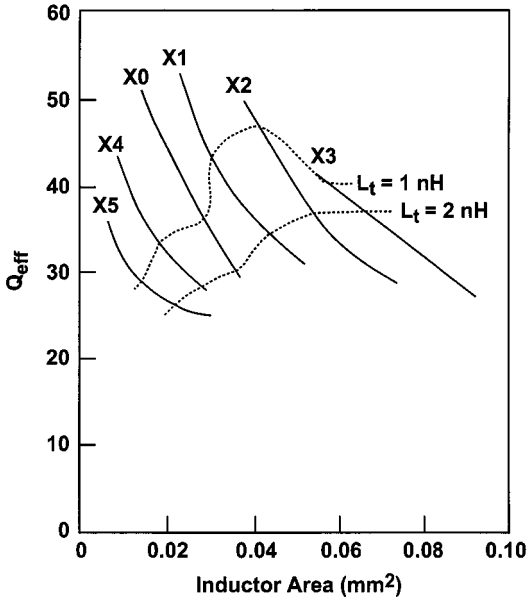

Fig. 6. Variations of measured $Q_{\rm eff}$ versus area for different inductors of type A.

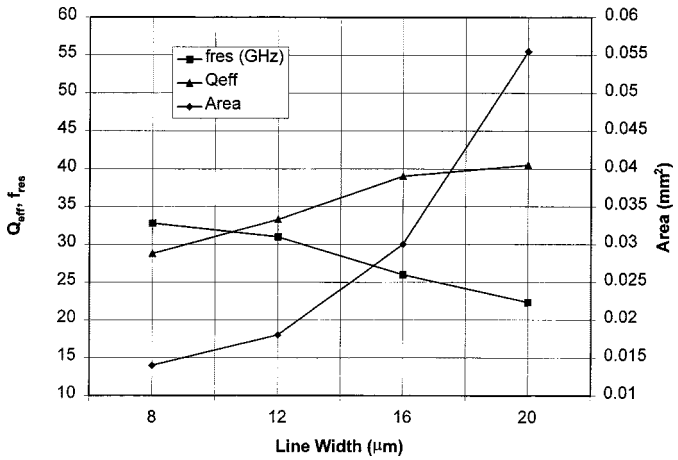

Fig. 8. Inductor's $Q_{\rm eff}$, $f_{\rm res}$ and area as a function of linewidth for 1-nH inductance value.

$X1$ have Di =108 and $n = 1.5$ $W = 20$ $S = 8$
n =2.5 $W = 16$ $S = 10$
n =3.5 $W = 12$ $S = 14$
$X2$ have Di =158 and $n = 1.5$ $W = 20$ $S = 8$
n =2.5 $W = 16$ $S = 10$
n =3.5 $W = 12$ $S = 14$
$X3$ have Di =210 and $n = 1.5$ $W = 20$ $S = 8$
n =2.5 $W = 16$ $S = 10$
n =3.5 $W = 12$ $S = 14$

$X4$ have Di =50 $W = 12$ $S = 8$ $n = 1.5, 2.5, 3.5$
$X5$ have Di =50 $W = 8$ $S = 8$ $n = 1.5, 2.5, 3.5, 4.5, 5.5.$

All dimensions are in micrometers.

For 1-nH inductance value, the $X5$-type inductors have about four times less area than the $X3$-type inductors, whereas larger value inductors are about three times smaller. Fig. 6 shows the $Q_{\rm eff}$ values as a function of inductor area. The broken lines indicate the $Q_{\rm eff}$ values for 1- and 2-nH inductance values. It may be noted that for an inductor having about 1-nH value, $X2$–type inductors provide the maximum $Q_{\rm eff}$, whereas for 2-nH value $X2$– and $X3$–type have similar $Q_{\rm eff}$ values, while $X3$–type inductors have about 25% larger area. Fig. 7 shows the self-resonant frequency of these inductors as a function of

TABLE IV
INDUCTOR PARAMETERS FOR SEVERAL INDUCTORS FABRICATED USING A MULTILEVEL MMIC PROCESS ON 75-μm-THICK GaAs SUBSTRATE

Inductor #	Width (μm)	Spacing (μm)	L_t (nH)	f_{res} (GHz)	Peak Q_{eff}
1.5I4A	12	8	0.342	>40	41.5
2.5I4A	12	8	0.808	34.2	35
3.5I4A	12	8	1.593	20.5	30
3.7I4A*	12	8	1.82	18.0	29
3.5I0A	12	14	1.82	18.7	30
3.5I1A	12	14	2.63	14.0	31.5
3.5I2A	12	14	3.63	10.6	29.5
3.5I3A	12	14	4.59	8.75	27.5

*** Extrapolated from Figs. 5,6 and 7.**

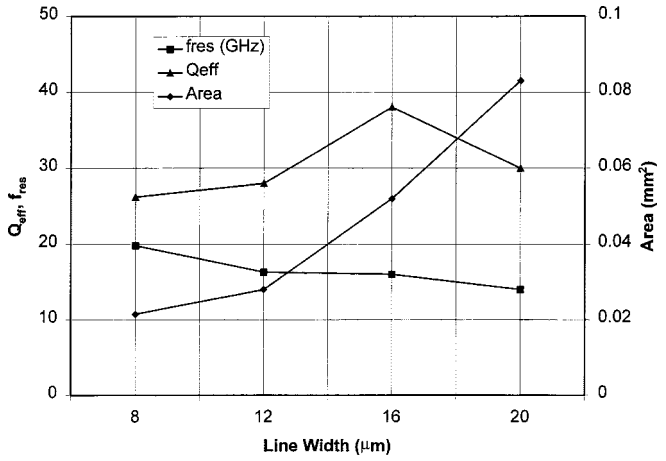

Fig. 9. Inductor's $Q_{\rm eff}$, $f_{\rm res}$ and area as a function of linewidth for 2-nH inductance value.

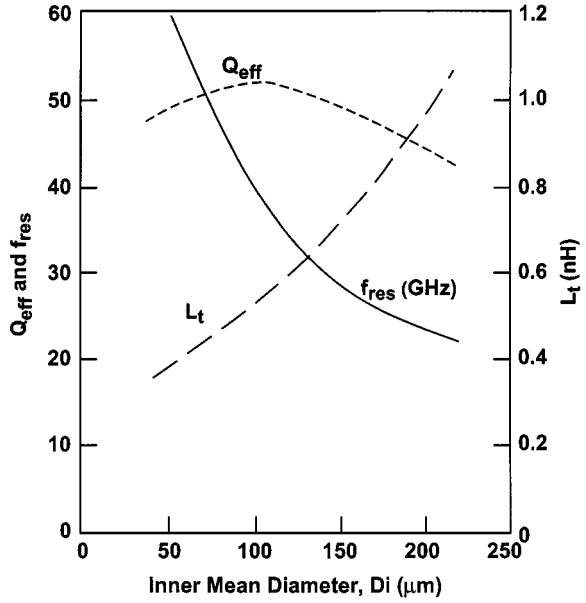

Fig. 10. Inductor's L_t, $Q_{\rm eff}$, and $f_{\rm res}$ versus inner mean diameter for 1.5-turn inductors.

area. The broken lines indicate the resonant frequency values for 1- and 2-nH inductance values. In general, the larger the area, the lower is the resonant frequency, and $X3$-type inductors have the lowest and $X5$–type inductors have the highest resonant frequencies.

A. Linewidth

The linewidth is the most critical variable in the design of coils. In general, the $Q_{\rm eff}$ factor increases due to lower dc resistance and $f_{\rm res}$ decreases due to higher parastic capacitance with the increase of linewidth. Figs. 8 and 9 show the variations of $Q_{\rm eff}$, $f_{\rm res}$, and inductor area for 1- and 2-nH inductance values, respectively. For $W = 8$ μm: $S = 8$ μm, $Di = 50$ μm and the variable is the number of turns. For $W = 12$ μm: S, Di, and n are variables. For $W = 16$ μm: $S = 10$ μm and Di and n are variables, whereas for $W = 20$ μm: $S = 8$ μm and Di and the number of turns are variables. For the 1-nH inductor, the increase in $Q_{\rm eff}$ value is not significant when the linewidth increases from 16 to 20 μm, while the increase in area is about 80%. For higher inductance values, an optimum linewidth is about 16 μm for the maximum $Q_{\rm eff}$ factor realization. The variable linewidth [24], [25] may also be used to improve the $Q_{\rm eff}$ factor in addition to several other techniques, as discussed in the literature [26]–[28].

B. Spacing Between Turns

In general, the $Q_{\rm eff}$-factor increases with the area of an inductor. However, small-area inductors mandate small separation between the turns. Table IV shows inductors parameters for 8- and 14-μm spacing. As expected, the 3.5I0A inductor has slightly higher inductance and lower $f_{\rm res}$ than 3.5I4A due to increased area. Since the 3.5I0A inductor has higher inductance and lower $f_{\rm res}$, it is expected that its $Q_{\rm eff}$ should be higher than the 3.5I4A inductor's $Q_{\rm eff}$. The data in Figs. 5–7 have been used

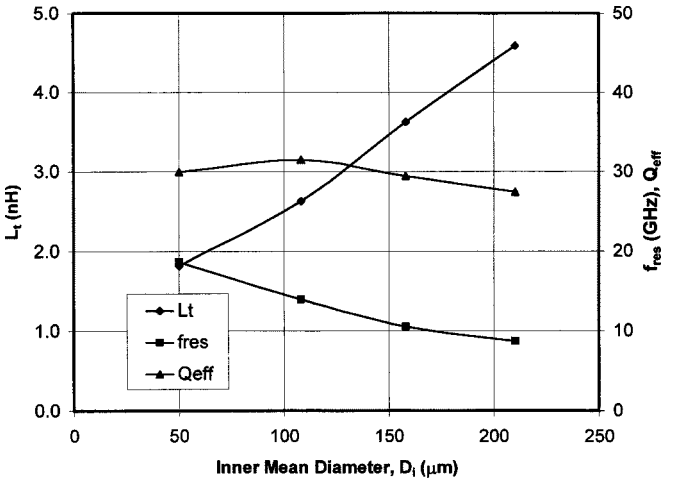

Fig. 11. Inductor's L_t, $Q_{\rm eff}$, and $f_{\rm res}$ versus inner mean diameter for 3.5-turn inductors.

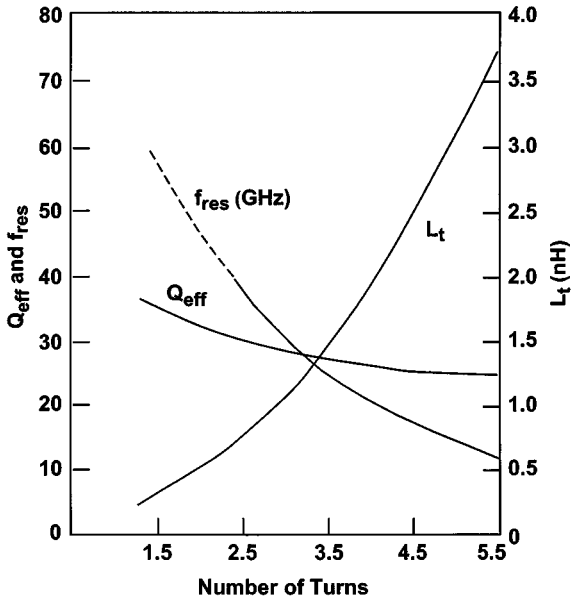

Fig. 12. Variations of L_t, $Q_{\rm eff}$, and $f_{\rm res}$ area function of number of turns for $X5$ inductors.

to extrapolate $f_{\rm res}$ and $Q_{\rm eff}$ values for the inductance value of 1.82 nH. As expected, the 3.7I4A inductor has lower $f_{\rm res}$ and $Q_{\rm eff}$ values than the 3.5I0A inductor.

C. Inner Diameter

Since the contribution of the innermost turn is low, due to a very small inner diameter, enough empty space must be left in the center of coil to allow the magnetic flux lines to pass through it in order to increase the stored energy per unit length. We designed inductors with four different inner diameters (50, 108, 158, and 210 μm). Figs. 10 and 11 show the variations of L_t, $Q_{\rm eff}$, and $f_{\rm res}$ as a function of inner diameter for $W = 20$ μm, $S = 8$ μm, $n = 1.5$, and $W = 12$ μm, $S = 14$ μm, $n = 3.5$, respectively. As expected, the inductance increases and $f_{\rm res}$ decreases with increasing inner diameter (D_i) due to

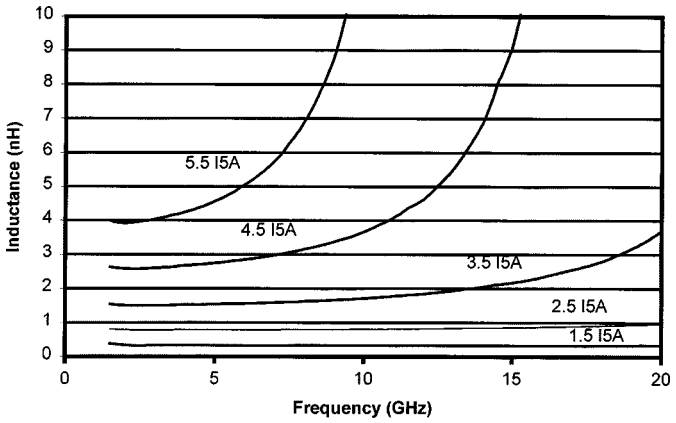

Fig. 13. Typical variations of L_t versus frequency for different inductor turns.

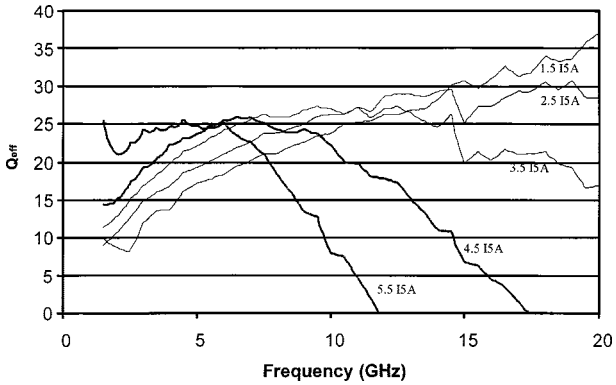

Fig. 14. Typical variations of $Q_{\rm eff}$ factor versus frequency for different inductor turns.

increased inductor area. As can be seen, the maximum $Q_{\rm eff}$ occurs around $D_i = 100$ μm. Similar optimum D_i is obtained for other linewidths and multilayer inductors.

D. Number of Turns

Multiturn inductors have higher inductance per unit area, but due to higher parasitic capacitances, have lower self-resonance frequencies. Fig. 12 shows the plots of L_t, $Q_{\rm eff}$, and $f_{\rm res}$ versus the number of turns for $\times 5$ inductors. The decrease of $Q_{\rm eff}$ with an increasing number of turns is because of increased parasitic capacitance and increased RF resistance due to eddy currents. Figs. 13 and 14 show typical variations of inductance and the $Q_{\rm eff}$ factor as a function of frequency for 1.5-, 2.5-, 3.5-, 4.5-, and 5.5-turn inductors. Data is shown up to first resonance. The maximum $Q_{\rm eff}$ point decreases with the increase of number of turns because of increased RF resistance due to eddy current and increase of parasitic capacitance. Below the maximum $Q_{\rm eff}$ point, the inductive reactance and $Q_{\rm eff}$ increase with frequency, while at frequencies above the maximum $Q_{\rm eff}$ point, the RF resistance increases faster than the inductive component. This results in decrease in the $Q_{\rm eff}$ value with frequency and $Q_{\rm eff}$ becomes zero at the resonance of the inductor. As expected, the inductance increases approximately as n^2, where n is the number of turns. For the $X5$–type inductors, the value of total inductance (in nanohenry), $Q_{\rm eff}$ factor, and resonance frequency (in

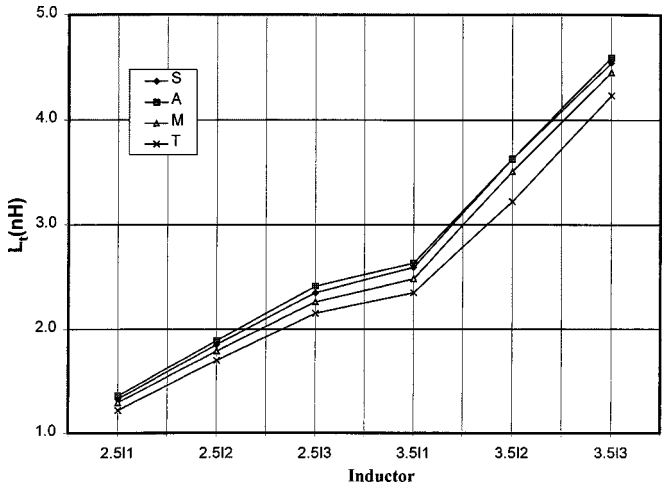

Fig. 15. Comparison of L_t for various inductors types fabricated using standard—S, multilayer—A, multilayer and multilevel metallization—M, and multilayer and multilevel thick metallization—T processes. For inductor parameters, refer to Tables I and II.

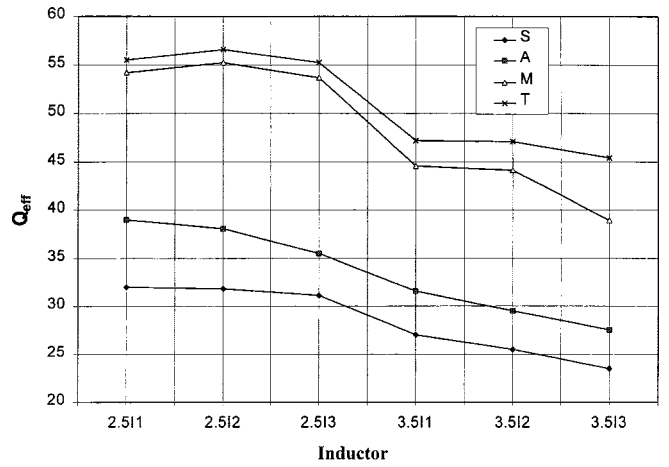

Fig. 16. Comparison of $Q_{\rm eff}$ for various inductors types fabricated using standard—S, multilayer—A, multilayer and multilevel metallization—M, and multilayer and multilevel thick metallization—T processes. For inductor parameters refer to Tables I and II.

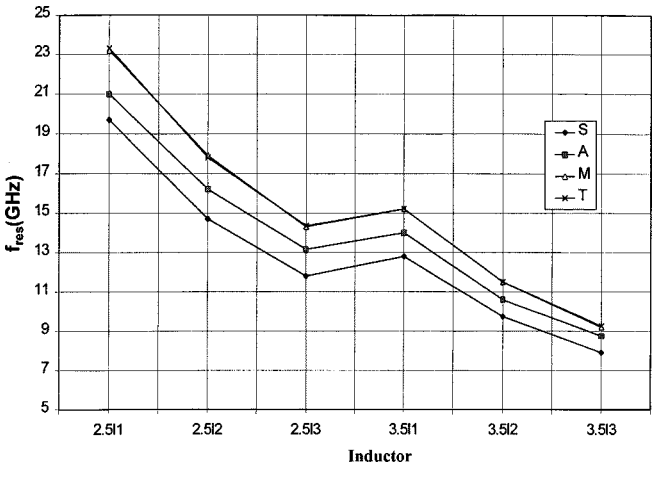

Fig. 17. Comparison of $f_{\rm res}$ for various inductors types fabricated using standard—S, multilayer—A, multilayer and multilevel metallization—M, and multilayer and multilevel thick metallization—T processes. For inductor parameters, refer to Tables I and II.

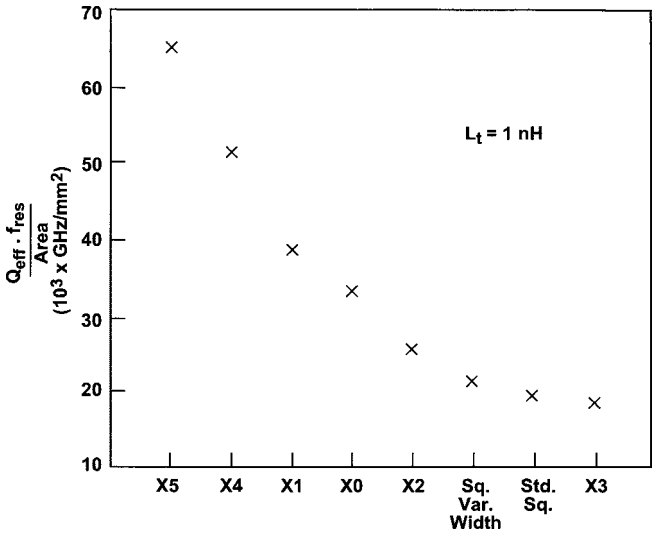

Fig. 18. Comparison of FMI for various inductors.

gigahertz) may be approximately calculated using the following empirical equations:

$$L_t = 0.04 + 0.12n^2 \tag{10}$$

$$Q_{\rm eff} = \frac{38}{n^{0.25}} \tag{11}$$

$$f_{\rm res} = \frac{36.52}{0.9432 + 0.01n^{3.15}}, \qquad \text{for} \quad < 30\ \text{GHz} \tag{12}$$

E. Multilayer Inductors

Typical inductance values for MMIC applications on a GaAs substrate in the microwave frequency band fall in the range from 0.2 to 10 nH. On a thin GaAs substrate (3 mil or smaller), the use of high value inductors in the matching networks becomes difficult because of lower resonant frequencies due to inter-turn fringing capacitance and shunt capacitance to ground. These parasitic capacitances can be reduced significantly by using a multilayer configuration [29].

Several type of multilayer inductors have been tested and compared with standard inductors. Variations of L_t ($L + L_1 + L_2$), the Q factor $Q_{\rm eff}$, and resonance frequency ($f_{\rm res}$) for four inductor types (see Table I for designation) are shown in Figs. 15–17, respectively. In comparison to the standard inductors, the inductors using multilayer process have about 17%–21% higher resonance frequency and 65%–73% higher $Q_{\rm eff}$ factor values. The thicker polyimide layer increases the values of the $Q_{\rm eff}$ factor and the resonance frequency of the inductors due to reduced dissipated loss and lower parasitic capacitance similar to the characteristics observed in multilayer microstrip data [29]. Similar improvements in the inductor's performance have also been observed by placing inductor

TABLE V
INDUCTOR PARAMETERS FOR SEVERAL VALUES OF POLYIMIDE THICKNESSES AND METALLIZATION THICKNESSES

Polyimide Thickness (μm)	Inductor #	L_t (nH)	Peak Q_{eff}	f_{res} (GHz)
0	2.5I3S	2.35	31.1	11.8
3	2.5I3A	2.41	35.5	13.15
10	2.5I3M	2.26	53.7	14.3
10	2.5I3T	2.15	55.2	14.35

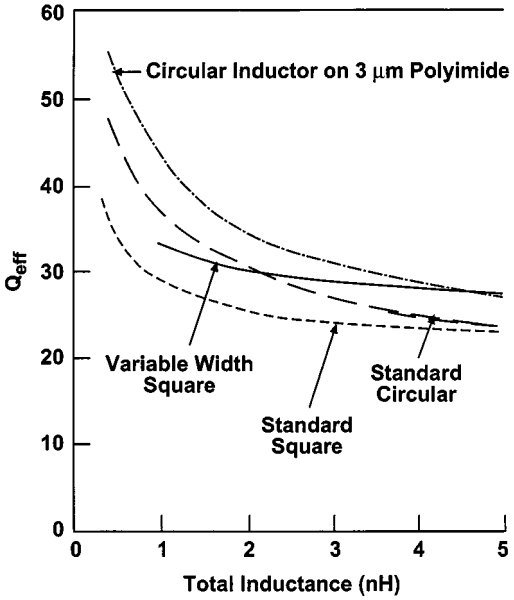

Fig. 19. Comparison of $Q_{\rm eff}$ for type A, and standard circular-, square-, and variable-width inductors.

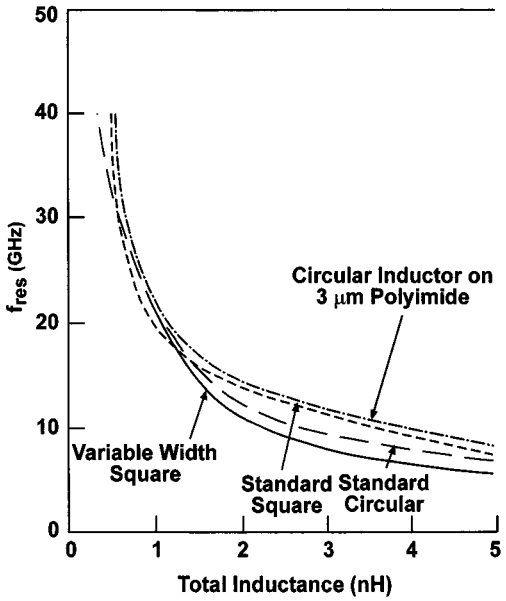

Fig. 20. Comparison of $f_{\rm res}$ for type A, and standard circular-, square-, and variable-width inductors.

conductor on thick oxidized porous silicon [18]. The total inductance value is more or less invariant.

F. Thickness Effect

We also investigated the effect of metal 2 (Fig. 2) thickness on the inductors characteristics. The Q factor of an inductor is increased by increasing the conductor thickness as it reduces the series resistance. For this study, we increased the thickness from 4.5 to 9.0 μm. This increases the current handling by a factor of two when the width of metal 1 is twice the inductor's linewidth (Table I). In the thick metallization case, the $Q_{\rm eff}$ value is further enhanced by about 3%–17%, the inductance value decreased by about 4%–6% and the resonant frequency did not change due to increased parasitic capacitance, as shown in Figs. 15–17. Table V summarizes the inductor model parameters for several 2.5-turn inductors. These inductors have up to 93% higher $Q_{\rm eff}$ factor values than the standard inductors.

G. Inductor Area

The Q factor of a coil may be enhanced by increasing its area using either larger inside diameter or wider line dimensions or by increasing the separation between the turns. In general, a wider line dimension reduces the dc resistance of the coil. However, the parasitic capacitance of the inductor trace and the RF resistance due to eddy current increase with the linewidth and sets the maximum limit for the linewidth. For a micromachined inductor, this limit is about 20 μm [24], whereas for planar inductors on a 3-mil-thick GaAs substrate, this limit is about 16 μm for larger inductance values.

However, for low-cost considerations, one needs compact inductors. Fig. 18 shows the figure-of-merit for several inductors of type A. The value of inductance chosen is 1 nH. It may be noted that the $X5$ structure has the best FMI because of the smallest area and highest resonance frequency due to lower parasitic capacitances.

The data presented in this paper for circular spiral inductors is also compared with the standard [28] and variable linewidth [25] square inductors in Figs. 19 and 20. As expected, the square inductors have lower $Q_{\rm eff}$ than the circular inductors; however, for higher values of inductances, the $Q_{\rm eff}$ values for the circular inductor on a 3-μm polyimide and the variable linewidth square inductors are comparable. The resonant frequencies for small

inductance values are comparable; however, for high values of inductance, the circular inductors have higher resonant frequencies, primary due to small linewidths.

VI. Conclusion

Several types of circular coil inductors were designed, fabricated, tested, modeled, analyzed, and compared. We developed high Q_{eff} and compact multilayer inductors having high current handling capacity for MMICs on GaAs substrates. In our experiments, we have demonstrated increased Q_{eff} factor by up to 93%; however, by optimizing the inductor's layout, the Q factor of planar spiral inductors may further be increased. The results of our finding can be summarized as follows. For a higher inductance value, one generally needs larger inner diameter, smaller linewidth, larger spacing, and a larger number of turns. For a given value of inductance, larger inner diameter, larger linewidth, and a smaller number of turns result in higher Q_{eff}, whereas smaller inner diameter, smaller linewidth, larger gap, and a larger number of turns are desired for higher f_{res}. On the other hand, compact size requires small inner diameter, small linewidth, small spacing, and a larger number of turns. Inductors of $X5$ type are a good compromise between the performance and size. Thicker conductors improve the current handling capacity, reduce the RF resistance without making variable linewidth [24], [25], and increase the resonant frequency of coil inductors. The performance of these inductors can be further improved by using low dielectric constant $(\varepsilon_r = 2.7)$ and low loss $(\tan\delta = 0.0006)$ benzocyclobutene (BCB) as a multilayer dielectric. The thermal resistance of polyimide or BCB is about 200 times the thermal resistance of GaAs. In order to ensure the reliable operation of these components for high-power applications, these components must be thermally modeled.

The use of compact multilayer (10-μm-thick polyimide) inductors in passive and active MMICs will result in improved RF performance, smaller size, and lower cost. These inductors can also be used as RF chokes for biasing power-amplifier circuits. The multilayer inductors also allow to use thinner (2–3 mil) GaAs substrates, which help in the reliability of the GaAs power ICs without increasing attenuation loss in the circuits.

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From 1969 to 1981, he performed research in parametric amplifiers, p-i-n diode phase shifters, microwave and millimeter-wave ICs, printed antennas, phased-array antennas, millimeter-wave antennas and medical and industrial applications of microwaves. Prior to joining ITT GaAsTEK (now M/A-COM Inc.), Roanoke VA, he spent five months at the Defense Research Establishment, Ottawa, ON, Canada, as a Research Scientist involved with millimeter-wave systems. In 1981, he joined the ITT Gallium Arsenide Technology Center, where, since that time, has been involved with microwave and millimeter-wave GaAs ICs. He has been directly responsible for the design of over 250 MMICs, including low-noise amplifiers, broad-band amplifiers, power amplifiers (high-power, high-efficiency, and broad-band), dc- and ac-coupled transimpedance and limiting amplifiers, multibit phase shifters, narrow-band and broad-band single-pole double-throw (SPDT) switches, redundant switches, programmable attenuators, balanced mixers, quadrature downconverters, upconverters, transmit chips, receive chips, and transmit/receive chips. He developed modules consisting of MMICs for phased-array radar (PAR) and electronic counter measure (ECM) applications. In his current capacity as an Executive Scientist with M/A-COM Inc., his interests are in the area of device modeling, high-efficiency high-power amplifiers, three-dimensional (3-D) MMICs, and development of MMIC products for commercial and military applications. He has authored or co-authored over 130 research papers. He has also authored *Microstrip Lines and Slotlines* (Norwood, MA: Artech House, 1979), *Microstrip Antennas* (Norwood, MA: Artech House, 1980), *Millimeter Wave Engineering and Applications* (New York: Wiley, 1984), *Microwave Solid State Circuit Design* (New York: Wiley, 1988), *Microstrip Lines and Slotlines, 2nd ed.* (Norwood, MA: Artech House, 1996), *RF and Microwave Coupled-Line Circuits* (Norwood, MA: Artech House, 1999), and *Microstrip Antenna Design Handbook* (Norwood, MA: Artech House, 2001), and co-edited *Microwave and Millimeter-Wave Heterostructure Transistors and Their Applications* (Norwood, MA: Artech House, 1989) and *Gallium Arsenide IC Applications Handbook* (New York: Academic, 1995). He has also contributed two chapters to the *Handbook of Microwave and Optical Components* (New York: Wiley, 1989), one chapter to the *Handbook of Electrical Engineering* (Boca Raton, FL: CRC Press, 1997), three chapters to the *Gallium Arsenide IC Applications Handbook* (New York: Academic, 1995) and one chapter to the *Wiley Encyclopedia of Electrical and Electronics Engineering, Vol. 13* (New York: Wiley, 1999). He holds 15 patents in the areas of microstrip antennas and microwave circuits. He is an Editorial Board member for *Microwave Optical Technology Letters* and *Microwave Journal*. He is also an Associate Editor for the *International Journal of RF and Microwave Computer-Aided Engineering*.

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